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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,891	08/11/2004	Yuan-Ting Wu	MTKP0088USA	4890
27765	7590	02/11/2008		
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116				EXAMINER THAMMAVONG, PRASITH
			ART UNIT 2187	PAPER NUMBER
			NOTIFICATION DATE 02/11/2008	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)
	10/710,891	WU ET AL.
	Examiner	Art Unit
	Prasith Thammavong	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 September 2007.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 23-42 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 23-42 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 17 September 2007 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 9/17/07. At this point claims 1-22 have been cancelled; and claims 23-42 have been added. Thus, claims 23-42 are pending in the instant application.

The instant application having Application No. 10/710,891 has a total of 20 claims pending in the application, there are 4 independent claims and 16 dependent claims, all of which are ready for examination by the examiner.

1. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

2. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by M.P.E.P. ' 201.14(c), acknowledgment is made of applicant's claim for priority based on an application filed 9/8/2003 in Taiwan.

3. REJECTIONS NOT BASED ON PRIOR ART

a. DEFICIENCIES IN THE CLAIMED SUBJECT MATTER

Claim Rejections - 35 USC ' 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 23, the term "substantially equal" on line 6 is a relative term which renders the claim indefinite. The term "substantially equal" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For examination purposes, the Examiner has construed the term "substantially equal" to mean equal or not equal. **Claims 26, 28, 31, 33, 36, 38 and 41** suffer from a similar deficiency as claim 23.

With respect to claim 24, the term "normal operations" on line 6 is a relative term which renders the claim indefinite. The term "normal" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For examination purposes, the Examiner has construed the term "normal operations" to mean any type of operations. **Claims 29, 34, and 39** suffer from a similar deficiency as claim 24.

With respect to claim 28, line 6 recites "the shifted memory address space being shifted by an amount being substantially equal to the size of the memory section to be protected **to thereby move the memory section to be protected outside of the shifted memory address space".** (**emphasis added**) It is unclear to the Examiner on how "the memory section to be protected" is moved "outside the shifted memory address space" when "the memory section to be protected" has not changed location in the memory. For Examination purposes, the Examiner has construed that the memory addresses in "the shifted memory space" can not access "the memory section to be

protected" as it "outside" of the address space of the "the memory section to be protected". **Claim 38** suffers from a similar deficiency as claim 28.

Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: how the shifted memory address space is generated. Line 5-8 recites "**generating a shifted memory address space of the memory, the shifted memory address space being shifted by an amount being substantially equal to the size of the memory section to be protected** to thereby move the memory section to be protected outside of the shifted memory address space". (**emphasis added**) It is unclear to the Examiner from what base address space, if any, "the shifted address space" is being generated from as it seems there "the shifted address space" is being shifted by an "an amount being substantially equal to the size of the memory section to be protected" *but does entail from where "the shifted address space" is being shifted from*. For Examination purposes, the Examiner has construed that there could or could not be a base address space that "the shifted address space" is being shifted from.

Claim 38 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: a "generated shifted memory address space" and from what address space is being shifted to generate the "shifted memory address space. Line 5-9 recites "**generating a shifted**

memory address space of the memory, the shifted memory address space being shifted by an amount being substantially equal to the size of the memory section to be protected to thereby move the memory section to be protected outside of the shifted memory address space". (emphasis added) It is unclear to the Examiner from what base address space, if any, "the shifted address space" is being generated from as it seems there "the shifted address space" is being shifted by an "an amount being substantially equal to the size of the memory section to be protected" *but does entail from where "the shifted address space" is being shifted from.* For Examination purposes, the Examiner has construed that there could or could not be a base address space that "the shifted address space" is being shifted from.

Claim 38 suffers from a similar deficiency as claim 28.

Any dependent claims inherit all the deficiencies of their respective parent claim.

4. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC '102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 23-25, 28-30, 33-35, and 38-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasbun (US Patent # 6,205,548).

With respect to claim 23, the Hasbun reference teaches a method of protecting a memory section from being accessed, the method comprising:

providing a memory (see fig. 3, element 340) being coupled to a microprocessor (see fig. 3, element 330), the memory having a memory section to be protected of a particular size; (column 5, lines 25-37, where there is a memory which has a block that is locked)

generating a first memory address by the microprocessor for accessing the memory; (column 5, lines 38-42, where the processor requests information at a particular address)

shifting the first memory address by an amount being substantially equal to the size of the memory section to be protected to thereby generate a shifted memory address being different from the first memory address; (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344) and

accessing the memory utilizing the shifted memory address for all memory accesses by the microprocessor when it is desired to prevent the memory section from being accessed by the microprocessor. (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed)

With respect to claim 24, the Hasbun reference teaches preventing the memory section from being accessed during normal operations of the microprocessor by coupling the shifted memory address to the memory immediately after the

microprocessor has finished booting, and continually coupling the shifted memory address to the memory for all subsequent normal operations of the microprocessor. (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed, and when block 344 should be used for boot code)

With respect to claim 25, the Hasbun reference teaches:

storing boot code for the microprocessor in the memory section; (column 6, lines 31-44, where the blocks can be used to store boot code) and
booting the microprocessor utilizing the boot code stored in the memory section by coupling the first memory address to the memory before the microprocessor begins booting and while the microprocessor is booting. (column 6, lines 31-44, where the blocks can be used to store boot code, and the processor uses the boot code to boot the system)

With respect to claim 28, the Hasbun reference teaches a method of protecting a memory section from being accessed, the method comprising:

providing a memory (see fig. 3, element 340) being coupled to a microprocessor (see fig. 3, element 330), the memory having a memory section to be protected of a particular size; (column 5, lines 25-37, where there is a memory which has a block that is locked)

generating a shifted memory address space of the memory, the shifted memory address space being shifted by an amount being substantially equal to the size of the memory section to be protected to thereby move the memory section to be protected

outside of the shifted memory address space; (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344) and

accessing the memory utilizing shifted memory addresses being within the shifted memory address space for all memory accesses by the microprocessor when it is desired to prevent the memory section from being accessed by the microprocessor. (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed)

With respect to claim 29, the Hasbun reference teaches preventing the memory section from being accessed during normal operations of the microprocessor by coupling the shifted memory addresses of the shifted memory address space to the memory immediately after the microprocessor has finished booting, and continually coupling the shifted memory addresses to the memory for all subsequent normal operations of the microprocessor. (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed, and when block 344 should be used for boot code)

With respect to claim 30, the Hasbun reference teaches generating the shifted memory address space includes shifting an original memory address space of the memory by the amount being substantially equal to the size of the memory section to be protected, (column 6, lines 3-21, where the address decoder receives an address for

block 342 and the address received can be remapped to block 344 when block 342 should not be accessed) and the method further comprises:

storing boot code for the microprocessor in the memory section; (column 6, lines 31-44, where the blocks can be used to store boot code) and
booting the microprocessor utilizing the boot code stored in the memory section by coupling un-shifted memory addresses in the original memory address space to the memory before the microprocessor begins booting and while the microprocessor is booting. (column 6, lines 31-44, where the blocks can be used to store boot code, and the processor uses the boot code to boot the system)

With respect to claim 33, the Hasbun reference teaches an electronic system comprising:

a memory (see fig. 3, element 340) having a memory section of a particular size to be protected; (column 5, lines 25-37, where there is a memory which has a block that is locked)

a microprocessor (see fig. 3, element 330) being coupled to the memory, for generating a first memory address for accessing the memory; (column 5, lines 38-42, where the processor requests information at a particular address) and

an address translator (see fig. 3, element 320) being coupled between the microprocessor and the memory, for shifting the first memory address by an amount being substantially equal to the size of the memory section to be protected to thereby generate a shifted memory address being different from the first memory address;

(column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344)

wherein the shifted memory address outputted by the address translator is coupled to the memory for all memory accesses when it is desired to prevent the memory section from being accessed by the microprocessor. (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed)

With respect to claim 34, the Hasbun reference teaches wherein the address translator is further for preventing the memory section from being accessed during normal operations of the microprocessor by coupling the shifted memory address to the memory immediately after the microprocessor has finished booting, and continually coupling the shifted memory address to the memory for all subsequent normal operations of the microprocessor. (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed, and when block 344 should be used for boot code)

With respect to claim 35, the Hasbun reference teaches wherein the memory is further for storing boot code for the microprocessor in the memory section, and the microprocessor is further for booting utilizing the boot code stored in the memory section by coupling the first memory address to the memory before and during booting. (column 6, lines 31-44, where the blocks can be used to store boot code, and the processor uses the boot code to boot the system)

With respect to claim 38, the Hasbun reference teaches an electronic system comprising:

a microprocessor; (see fig. 3, element 330)

a memory(see fig. 3, element 340) being coupled to the microprocessor, the memory having a memory section of a particular size to be protected; (column 5, lines 25-37, where there is a memory which has a block that is locked)

an address translator (see fig. 3, element 320) for generating a shifted memory address space of the memory, the shifted memory address space being shifted by an amount being substantially equal to the size of the memory section to be protected to thereby move the memory section to be protected outside of the shifted memory address space; (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344)

wherein all memory accesses by the microprocessor access the memory utilizing shifted memory addresses being within the shifted memory address space when it is desired to prevent the memory section from being accessed by the microprocessor. (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed)

With respect to claim 39, the Hasbun reference teaches wherein the address translator is further for preventing the memory section from being accessed during normal operations of the microprocessor by coupling the shifted memory addresses of the shifted memory address space to the memory immediately after the microprocessor

has finished booting and by continually coupling the shifted memory addresses to the memory for all subsequent normal operations of the microprocessor. (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed, and when block 344 should be used for boot code)

With respect to claim 40, the Hasbun reference teaches wherein the address translator is further for shifting an original memory address space of the memory by the amount being substantially equal to the size of the memory section to be protected to thereby generate the shifted memory address space; (column 6, lines 3-21, where the address decoder receives an address for block 342 and the address received can be remapped to block 344 when block 342 should not be accessed, and when block 344 should be used for boot code)

the memory is further for storing boot code for the microprocessor in the memory section; (column 6, lines 31-44, where the blocks can be used to store boot code) and

the microprocessor is further for booting utilizing the boot code stored in the memory section by coupling un-shifted memory addresses in the original memory address space to the memory before and during booting. (column 6, lines 31-44, where the blocks can be used to store boot code, and the processor uses the boot code to boot the system)

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 26-27, 31-32, 36-37 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasbun (US Patent # 6,205,548) in view of Wisor (US Patent # 6,823,435).

With respect to claims 26 and 31, the Hasbun reference teaches:

shifting the first memory address by the value stored in the register to thereby generate the shifted memory address; (column 6, lines 3-21, where the boot selector value is used to determine which block is addressed) and

shifting the first memory address by a new value stored in the register to thereby generate a new shifted memory address. (column 6, lines 3-21, where the boot selector value is used to determine which block is addressed)

The Hasbun reference does not explicitly teach:

storing a value being substantially equal to the size of the memory section to be protected in a register;

changing the size of the memory section to be protected to a new size after updating contents of the memory section;

changing the value stored in the register to a new value corresponding to the new size of the memory section to be protected;

However, the Wisor reference teaches:

storing a value being substantially equal to the size of the memory section to be protected in a register; (column 6, lines 24-35, where the configuration register stores size information about the boot code section)

changing the size of the memory section to be protected to a new size after updating contents of the memory section; (column 6, lines 43-57, where the size can be changed in the boot code section) and

changing the value stored in the register to a new value corresponding to the new size of the memory section to be protected. (column 6, lines 43-57, where the size in the configuration can be changed to be the same size of the boot code section)

The Hasbun and Wisor references are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the teaching of the Hasbun reference to:

store a value being substantially equal to the size of the memory section to be protected in a register;

change the size of the memory section to be protected to a new size after updating contents of the memory section; and

change the value stored in the register to a new value corresponding to the new size of the memory section to be protected, as taught by the Wisor reference.

The suggestion/motivation for doing so as it would be "beneficial to have a flash memory device wherein the size of the protected portion used to store the boot code may be programmably selected", as described by Wisor in column 4, lines 46-49.

Therefore, it would have been obvious to combine the teachings of the Hasbun reference with the Wisor reference for the benefit of boot code size modification as specified in claims 26 and 31.

With respect to claim 27, the Hasbun reference teaches wherein updating contents of the memory section further comprises storing updated boot code for the microprocessor in the memory section. (column 6, lines 31-44, where there is the boot code can be updated)

With respect to claim 32, the Hasbun reference teaches wherein updating contents of the memory section further comprises storing updated boot code for the microprocessor in the memory section. (column 6, lines 31-44, where there is the boot code can be updated)

With respect to claims 36 and 41, the Hasbun reference teaches:

wherein the address translator is further for shifting the first memory address by the value stored in the register to thereby generate the shifted memory address; (column 6, lines 3-21, where the boot selector value is used to determine which block is addressed)

the address translator is further for shifting the first memory address by a new value stored in the register to thereby generate a new shifted memory address. (column 6, lines 3-21, where the boot selector value is used to determine which block is addressed)

The Hasbun reference does not explicitly teach:

a register for storing a value being substantially equal to the size of the memory section to be protected;

and after updating contents of the memory section, the size of the memory section to be protected is changed to a new size; and

the register is further for storing a new value corresponding to the new size of the memory section to be protected.

However, the Wisor reference teaches:

a register for storing a value being substantially equal to the size of the memory section to be protected; (column 6, lines 24-35, where the configuration register stores size information about the boot code section)

and after updating contents of the memory section, the size of the memory section to be protected is changed to a new size; (column 6, lines 43-57, where the size can be changed in the boot code section) and

the register is further for storing a new value corresponding to the new size of the memory section to be protected. (column 6, lines 43-57, where the size in the configuration can be changed to be the same size of the boot code section)

The Hasbun and Wisor references are analogous art because they are from the same field of endeavor of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the teaching of the Hasbun reference to have:

a register for storing a value being substantially equal to the size of the memory section to be protected;

and after updating contents of the memory section, the size of the memory section to be protected is changed to a new size; and the register is further for storing a new value corresponding to the new size of the memory section to be protected, as taught by the Wisor reference.

The suggestion/motivation for doing so as it would be "beneficial to have a flash memory device wherein the size of the protected portion used to store the boot code may be programmably selected", as described by Wisor in column 4, lines 46-49.

Therefore, it would have been obvious to combine the teachings of the Hasbun reference with the Wisor reference for the benefit of boot code size modification as specified in claims 36 and 41.

With respect to claim 37, the Hasbun reference teaches wherein the memory section is further for storing updated boot code for the microprocessor. (column 6, lines 31-44, where there is the boot code can be updated)

With respect to claim 42, the Hasbun reference teaches wherein the memory section is further for storing updated boot code for the microprocessor. (column 6, lines 31-44, where there is the boot code can be updated)

5. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments with respect to claims 23-42 concerning the Kaiser reference have been considered but are moot in view of the new ground(s) of rejection.

However, Applicant's arguments with respect to claims 23-42 concerning the Hasbun reference have been considered but are not persuasive. See reasons below.

Applicant's Arguments pertaining to claim 23-27 and 33-37 on pages 11, 13, and 14:

In response to the argument that the Hasbun reference does not teach the limitation of "accessing the memory utilizing the shifted memory address for all memory accesses by the microprocessor when it is desired to prevent the memory section from being accessed by the microprocessor" on page 11, the Examiner respectfully disagrees.

The Examiner contends that the Hasbun reference teaches the limitation of "accessing the memory utilizing the shifted memory address for all memory accesses by the microprocessor when it is desired to prevent the memory section from being accessed by the microprocessor", as the Hasbun reference teaches that microprocessor 330 were to request an address of block 342 and if block 342 were locked, the address decoder 320 would translate the address of block 342 to the address of block 344 to allow access to block 344 and preventing access to block 342, which can be seen in column 5, lines 38-41 and column 6, lines 3-20.

In response to the argument that "swapping the addresses of two blocks in memory is not equivalent or similar to the present invention" on page 13, the Examiner respectfully disagrees with the interpretation of the applicant.

The Examiner also contends that the "swapping the addresses of two blocks in memory" is similar to the present invention as the translating above effectively "swaps" the address, but there is a translation in order to **effectively "swap"** the addresses which can be seen in column 6, lines 3-20 which states in part:

The **decoder translates** the first range of addresses **to access block 344 instead of block 342.** Any address in the second range of addresses will be decoded to access block 342. Thus toggling the value of the block selector **effectively remaps or swaps addresses** for blocks 342 and 344. (**emphasis added**)

In response to the argument that "Hasbun teaches (in col 5, line 64 to col 6, line 2), "... the address mapping to the other blocks remains unchanged"" on page 14, the Examiner respectfully disagrees with the interpretation of the applicant.

The Examiner contends even though reference of "Hasbun teaches (in col 5, line 64 to col 6, line 2), "... the address mapping to the other blocks remains unchanged".", this merely states the mapping of the other blocks (which are not apart of the booting process) can be accessed via the conventional means of addressing and are not apart of the booting process and thusly do not require that the addresses "remapped" or "swapped" within the booting process.

In response to the argument that "the teachings of Hasbun are still restricted to the block sizes of the memory which are determined at the time of manufacture" on page 14, the Examiner has included the USC 103 rejection of the Hasbun and Wisor reference to address these new claims as seen above.

Applicant's Arguments pertaining to claim 28-32 and 38-42 on pages 15-16:

In response to the argument that the Hasbun reference does not teach the limitation of shifting the memory address space "to thereby move the memory section to be protected outside of the shifted memory address space" on page 15 and that "swapping a subset (as taught by Hasbun) is not the same as moving an entire memory address space, as described in the present invention" on page 16, the Examiner respectfully disagrees. See reasons above pertaining to claims 23 and 33.

6. CLOSING COMMENTS

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. '707.07(i):

a(1) CLAIMS NO LONGER IN THE APPLICATION

Claims 1-22 were cancelled by the amendment dated 9/17/07.

a(2) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 23-42 have received a second action on the merits and are subject of a second action final.

b. **DIRECTION OF FUTURE CORRESPONDENCES**

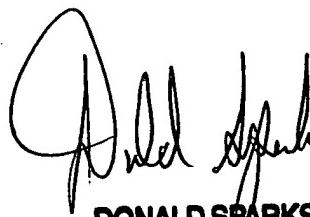
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasith Thammavong whose telephone number is (571) 270-1040 can normally be reached on Monday - Thursday 9:00am - 6:00pm and the first Friday of the bi-week, 9:00 am -5:00 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PT

Prasith Thammavong
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February 1, 2008



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